

AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A system for detecting transaction errors in ~~a~~ which the system comprising has a plurality of data processing devices ~~using~~ that use a common system interconnect bus, comprising:

a node controller operably coupled to ~~said~~ the system interconnect bus;

a plurality of interface agents ~~communicatively~~ operably coupled to ~~said~~ the node controller to have transactions with a source external to the system; and

an address table ~~comprising~~ coupled to the node controller and having a plurality of predetermined virtual ~~register~~ addresses that operate as dummy registers, wherein ~~said~~ the virtual addresses correspond to predetermined transaction error conditions, ~~but do not correspond to actual physical registers;~~

~~wherein errors corresponding to transactions between said interface agents and other processing modules in said system are directed to said node controller; and~~

~~wherein said node controller is operable to flag said errors using said predetermined virtual register addresses and to communicate said errors to said system interconnect bus for detection and wherein errors in the transactions through the interface agents are identified for predetermined transaction error conditions in the node controller and associated with corresponding addresses in the address table, so that the node controller is operable to flag the errors on the system interconnect bus for detection by the data processing devices by placing the virtual addresses on the system interconnect bus, in order to inhibit one or more data processing devices from generating additional error indications when processing the transactions.~~

2. (currently amended) The system of claim 1, wherein ~~said~~ the interface agents operate ~~in accordance with the~~ on data using a hypertransport protocol.

3. (currently amended) The system of claim 1, further comprising a system control and debug module operably ~~connected to said~~ coupled to the system interconnect bus to perform debug operations.

4. (currently amended) The system of claim 3, further comprising a trace cache operably ~~connected to said~~ coupled to the system control and debug module, wherein ~~said~~ errors are detected by ~~said trace cache and said~~ the system control and debug module are stored in the trace cache.

5. (currently amended) The system of claim 1, wherein ~~said~~ the node controller sends said transactions corresponding to said errors to predetermined register addresses corresponding to error conditions error indications to storage locations noted by the virtual addresses.

6. (currently amended) The system of claim ~~5~~ 1, wherein ~~said transactions corresponding to said errors comprise~~ the transactions are input/output transactions.

7. (currently amended) The system of claim ~~5~~ 1, wherein ~~said transactions corresponding to said errors comprise~~ the transactions are control commands.

8. (currently amended) The system of claim ~~5~~ 1, wherein ~~said transactions corresponding to said errors comprise a writes to memory addresses~~ the transactions are memory write commands.

9. (currently amended) The system of claim ~~5~~ 1, wherein ~~said transactions corresponding to said errors comprise reads from memory addresses~~ the transactions are memory read commands.

10. (canceled)

11. (currently amended) The system of claim ~~9~~ 4, wherein ~~in said~~ the trace cache ~~is programmable to store~~ only a predetermined set of errors corresponding to a specified diagnostic protocol.

12. (currently amended) A method for detecting transaction errors in which a system ~~comprising~~ has a plurality of data processing devices ~~using that use~~ a common system interconnect bus, comprising:

detecting an error corresponding to a transaction between an interface agent and ~~another processing module in said~~ at least one of the data processing devices in the system, in which the error is one of a plurality of predetermined error conditions for the system and the error is detected by a node controller coupled to the system interconnect bus;

associating the detected error with a virtual address from a plurality of predetermined virtual addresses stored in an address table, wherein the predetermined virtual addresses operate as dummy registers;

~~flagging said error using a predetermined virtual register address in an address table, wherein said predetermined virtual register address corresponds to a predetermined transaction error condition, but does not correspond to an actual physical register the error on the system interconnect bus for detection by the data processing devices by placing a corresponding virtual address on the system interconnect bus, in order to inhibit one or more data processing devices from generating additional error indications when processing the transaction; and~~

~~communicating said transaction error to said system interconnect bus for detection by a plurality of system modules coupled to said system interconnect bus storing the error as an error indication for debugging.~~

13. (currently amended) The method of claim 12, wherein a switch couples the node controller to the interface agent

~~said interface agent in operably connected to a switch;~~

~~said switch is operable connected to a node controller; and~~

~~said node controller is operably connected to said system interconnect bus.~~

14. (currently amended) The method of claim 13, wherein ~~said~~ the interface agent operates ~~in accordance with the~~ on data using a hypertransport protocol.

15. (canceled)

16. (currently amended) The method of claim ~~15~~ 12, wherein ~~said transactions corresponding to said errors comprise input/output transactions~~ the transaction is an input/output transaction.

17. (currently amended) The method of claim ~~15~~ 12, wherein ~~said transactions corresponding to said errors comprise control commands~~ the transaction is a control command transaction.

18. (currently amended) The method of claim ~~15~~ 12, wherein ~~said transactions corresponding to said errors comprise a writes to memory addresses~~ the transaction is a memory write transaction.

19. (currently amended) The method of claim ~~15~~ 12, wherein ~~said transactions corresponding to said errors comprise reads from memory addresses~~ the transaction is a memory read transaction.

20. (currently amended) The method of claim ~~15~~ 12, wherein ~~said errors communicated to said system interconnect bus are stored~~ further including storing the error indication in a trace cache.